A Novel Load Adaptive ZVS Auxiliary Circuit for PWM Three-Level DC–DC Converters

Abstract

Introduction:
Three-level dc–dc converters are used for dc–dc conversion with galvanic isolation when the input voltage is typically higher than 500 V dc. The key advantage of this topology compared to the conventional dc–dc full-bridge converter in high voltage applications is that the input dc voltage is split equally so that the peak voltage stress of the semiconductor devices and the dc bus capacitors are reduced to half of the input dc voltage. This facilitates the use of lower voltage rated semiconductor devices with optimized on-state resistance and smaller parasitic components especially the drain source capacitance of MOSFETs as compared to higher voltage rated devices.

One of the major industrial applications of three-level PWM dc–dc isolated converters is in powering network servers in datacenters and telecom devices from three-phase utility mains. In such ac–dc converters, intermediate dc bus at the output of the front-end PWM three-phase rectifier can be higher than 500 V so that three-level dc–dc PWM converter is an ideal
converter for accomplishing dc–dc conversion. Although there exists quite a few three-phase ac-to-dc rectifiers with input power factor correction (PFC), the PWM three-phase boost-type rectifier is one of the simplest and cheapest three-phase active rectifier which is often used in industrial converters for three-phase ac-to-dc power conversion with input PFC.

**Existing system:**

Traditional zero-voltage switching (ZVS) pulse width modulation (PWM) half-bridge (HB) TL dc/dc converters. It can realize ZVS for the power switches by making use of the parallel snubber capacitors or parasitic capacitors of the power switches and the leakage inductance of the transformer. Based on the traditional ZVS TL converter uses a tapped-inductor-type smoothing filter to replace the traditional smoothing filter.

**Proposed system:**

In order to overcome the issues associated with load adaptive ZVS in three-level PWM dc–dc converters, a new three-level converter topology is proposed in this paper. A simple load adaptive ZVS auxiliary circuit consisting of auxiliary inductors \( La1 \) and \( La2 \), dc bus-splitting capacitors \(Cb1, Cb2\), and flying capacitors \(Cb3\) and \(Cb4\), which are also involved in the voltage balancing mechanism along with clamping diodes \(Dc1\) and \(Dc2\). A dc blocking capacitor \(Cblk\) is
necessary to block any dc voltage in the transformer primary winding. The auxiliary windings $La_1$ and $La_2$ are magnetically coupled with an effective turns ratio of 1:1 and inductance of $LC$ are the key components of the auxiliary circuit.

### Advantages:

- Create an external current source by charging and discharging the coupled inductors which will be utilized for ZVS of the bridge devices from no-load to full load.
- The current in the ramp will reduce automatically with increasing load due to its unique magnetic coupling thus which is essential for reducing conduction losses from circulating currents and also optimize ZVS of the devices since at higher loads the converter can have natural ZVS.
Coupled inductor will lead to a smaller size of the auxiliary circuit due to the reduced volts-seconds and fewer components.

**Applications:**
- Telecom applications.

**Block diagram:**
Tools and software used:

- MPLAB – microcontroller programming.
- ORCAD – circuit layout.
- MATLAB/Simulink – Simulation.