A Low-Power Broad-Bandwidth Noise Cancellation VLSI Circuit Design for In-Ear Headphones

Abstract:

Conventional active noise cancelling (ANC) headphones often perform well in reducing the low-frequency noise and isolating the high-frequency noise by earmuffs passively. The existing ANC systems often use high-speed digital signal processors to cancel out disturbing noise, which results in high power consumption for a commercial ANC headphone. The contribution of this paper can be classified into: 1) proper filter length selection; 2) low-power storage mechanism for convolution operation; and 3) high-throughput pipelining architecture. With these novel techniques, we develop an area-/power-efficient ANC circuit by using the TSMC 90-nm CMOS technology for in-ear headphone applications. The proposed feed-forward filtered-x least mean square ANC circuit design provides the features of using lower operating frequency and consuming much less power that facilitate better performance than the conventional ANC headphones. To verify the effectiveness of the proposed design, a series of physical measurements is executed in an anechoic chamber. Measurement results show that the proposed high-performance/low-power circuit design can reduce disturbing noise of various frequency bands very well, and outperforms the existing works. The proposed design can attenuate 15 dB for broadband pink noise between 50 and 1500 Hz when operated at 20-MHz clock frequency at the costs of 84.2 k gates and power consumption of 6.59 mW only. Compared with the existing designs, the proposed work achieves higher noise cancellation performance in terms of 3 dB further and saves 97% power consumption. The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx 14.2.

Enhancement of the project:

Existing System:

The ANC applications often use the high-speed digital signal processors (DSPs) to carry out the active noise cancellation systems. For example, an active noise cancellation system in a long duct was realized on DSP platform to achieve real-time performance in attenuating the noise.
narrowband noise at low frequencies efficiently. The adaptive feedback ANC algorithm and its variations have been proposed for the ANC headphones to cancel out the narrowband noise at low frequencies. To effectively cancel the broadband noise for the ANC headphones, Guldenschuh and Höldrich exploit a prediction filter to replace the LMS algorithm. Hence, the system did not require real-time updates and became more robust against the acoustic changes. However, Guldenschuh and Höldrich mainly depend on the passive attenuation of the headphones. This is quite different from the target for in-ear headphones. A simple and effective approach for designing feedback controllers had been proposed, which attenuated the broadband noise effectively based on analyzing the waterbed effect of the feedback ANC system. Zhang and Qui study the causality issue on a feedforward ANC headphone with different directions of noise sources in free field so that the system can effectively cancel the broadband noise. Nevertheless, using DSP as a core component in the ANC systems, resulted in an expensive cost and high power dissipation. To reduce the cost for the ANC headphones, Chang and Li and Shyu et al. propose a modified feedback ANC algorithm and utilize a low-cost microcontroller unit as the core component in the ANC headphone. However, the noise cancelling performances of these systems become worse if the bandwidth of noise increases.

In addition to stereo audio channels and high-performance/low-power features, in-ear ANC headphones require stricter signal processing speed due to the physical constraints on the tiny volume. In this paper, a dedicated feedforward ANC circuit implementation based on the well-known FxLMS adaptive algorithm for high fidelity in-ear headphones is developed.

Disadvantages:

- Area coverage is high
- Power consumption is high

Proposed System:

A feed-forward ANC control system uses an input microphone close to the noise source to pick up the noise signal x(n) before it is sensed by the listener. Accordingly, the ANC controller can produce an antinoise signal y(n) processing equal amplitude but opposite phase of x(n). Such antinoise signal is used to drive the cancelling-loudspeaker to generate a cancelling sound that attenuates the primary acoustic noise in the ANC system. Fig. 1 shows the application of the feed forward FxLMS adaptive algorithm in ANC system, where P(z) and S(z), respectively, denote
the primary-path and the secondary-path models. In addition, \( W(z) \) indicates the filter weights of the ANC controller to adaptively generate the required antinoise signal according to the time-variant noise source.

**Fig. 1. Feedforward FxLMS algorithm**

**Proposed Hardware Architecture for the ANC In-Ear Headphone**

Fig. 2 shows the system architecture for implementing the proposed ANC system prototype where the proposed ANC architecture is shown in the bottom half of the figure.

As shown in Fig. 2, the proposed design contains the following submodules:

1) two 24-tap adaptive filters, i.e., LMS\(_{24\text{-tap}}\)\(W(z)\) for producing the antinoise signal \(y(n)\) and LMS\(_{24\text{-tap}}\)\(S(z)\) for estimating the secondary path online;

2) a finite-impulse response (FIR) filter, i.e., \(S(z)_{\text{FIR\_24\text{-tap}\_x}}(n)\), to produce the signal \(x(n)\) that is a filtered version of the signal \(x(n)\);

3) an adder for summing up the antinoise signal \(y(n)\) and the additive white noise used to keep track on the changes of \(S(z)\) due to small position variations of the in-ear headphone;

4) an I2S block in order to receive and transmit the data from the feedforward FxLMS ANC circuit to the I2S audio CODEC.
Fig. 2. Top-level block diagram of the system architecture.

The detailed hardware architecture of the proposed circular buffer is shown in Fig. 3, where the data buffer and coefficient buffer are used to store the data samples and filter coefficients, respectively. Two counters are equipped to drive the addresses of the data buffer and coefficient buffer. A comparator (Coeff addr == 22) controls the enable signal to disable the count for one cycle every output sample, and writes a new sample into the data buffer every 24 cycles.
Advantages:

- Area and power-efficient

Software implementation:

- Modelsim
- Xilinx ISE